**Computer Architecture 3rd Semester practical**

1. Implement the logic gates (AND, OR, NOT, NAND, NOR, XOR, XNOR) using VHDL and simulate the result for various combinations of input.
2. Implement the half adder using VHDL and simulate the result for various combinations of input.
3. Implement the full adder using VHDL and simulate the result for various combinations of input.
4. Implement the half subtractor using VHDL and simulate the result for various combinations of input.
5. Implement the full subtractor using VHDL and simulate the result for various combinations of input.
6. Implement the 4\*1 MUX using VHDL and simulate the result considering inputs and selection line.
7. Implement the 1\*4 DEMUX using VHDL and simulate the result considering inputs and selection line.
8. Implement the 3\*8 Decoder using VHDL and simulate the result considering the inputs.
9. Implement the 8\*3 Encoder using VHDL and simulate the result considering the inputs.
10. Implement the 4-bit binary parallel adder using VHDL and simulate the result considering the inputs.